Jingbin (Justin) Lin

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EDUCATION

University of California - San Diego
Master of Science in Computer Engineering (EC79)

Sept. 2025 – Present
California

McMaster University
Bachelor of Engineering in Electrical Engineering & Management

Sept. 2020 – June 2025
Canada

SKILLS

Languages : Verilog, C++, Python, TypeScript
Tools : Synopsys Design Compiler, Cadence Innovus, Virtuoso/AMS, ModelSim, Quartus Prime, Altium Designer, GitHub, Jira, Pytorch
Devices : Raspberry Pi, NVIDIA Jetson, Oscilliscope, Microscope, Soldering Station
Design Libraries : Generic 90nm Process Design Kit, FreePDK 45, TSMC 65 nm process PDK

AWARDS

- Dean's Honour List (2025, 2023, 2021)
- McMaster Honour Award (2020)
- Dr. Rudolf De Buda Scholarship (2025)

PROJECTS

Dual-Core Attention Accelerator
- RTL for dual MAC cores implementing the $QK^\top$ normalize pipeline for **Transformer** inference
- Designed **pmem**-centric accumulation and fixed-point **softmax** hardware blocks
- Executed workflow: **Synopsys Design Compiler** (synthesis), **Cadence Innovus** (hierarchical PnR), **Cadence AMS/Virtuoso**, and gate-level **VCD** simulation

2-D Systolic Array Design with CNN Implementation
- RTL for a **2D systolic array** supporting output- and weight-stationary CNN modes with local buffering
- Brought up the design on **Cyclone IV GX** FPGA, profiling power/throughput and tuning **multi-tiling** plus clock-gated datapaths
- Explore optimization like **SIMD**, **Clock Gating** and **multi-tiling** design

FIR Filter Adder Optimization on ASIC Design
- Modeled ripple, carry-save, and **Brent–Kung** prefix adders in **FIR** datapaths; captured activity via **ModelSim** for synthesis estimates
- Generated **Agilex 7** area/timing reports to justify the selected prefix + ripple-tail architecture for lower fanout and power

Wearable Cave Mapping System
- Led **PCB** design (power regulation, high-speed buses, MCU control) for a head-mounted 3D scanner
- Integrated **IMU**, **LiDAR**, and **Depth Camera** modules; validated 15 fps mapping over 3-hour battery runs

CMOS Differential Amplifier Design with AB Output Buffer
- Designed a differential Amplifier with AB buffer, meeting CMRR and bandwidth targets
- Ran AC/transient sims with **Virtuoso** to tune phase margin

WORK EXPERIENCE

MediumAI
Co-Founder&Software Engineer (@MediumAI)

Jan. 2023 – Present
Canada

- Built production RAG LLM pipelines for multilingual medical transcription and documentation
- Led R&D planning and delivery using **GitHub** and **Jira**
- Containerized services with **Docker**, orchestrated deployments with **Kubernetes**, and deployed to **Azure** (AKS); maintained CI/CD

Sun Yat-sen University
Computer Science RA Intern

May – August. 2023
China

- Developed neural-network models for physics simulation and differential equation solving
- Processed and visualized 3D scan datasets using **Open3D** and **Paraview**